

SHEET INDEX

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SYMBOL
BUFFER 0
ELEMENT IDENT

TECH. MOD.	FUNCTION	TERM.	LOC.
CLC01	I	012	280
CLC11	I	115	287
1AC10	I	176	283
LO00	I	014	284
BFCL11	I	210	282
BNCL10	I	309	282
SO100	I	015	283
-17.20V	I	016, 117	284
RACRO	#	197	295
RATACRO	#	006	292
BOC1	#	013	295
1500C1	#	016	295
SO170	#	114	296
SO170	#	238	297
-12V	#	210	284
+5	P	000, 119	290
GRD	G	200, 319	292

RECORD OF CHANGES

DWG	PREV	STD	MR	SEE
ISS	FURN		DISC	NOTE
241	2	Y	2	

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IK

CURRENT DRAIN: +5V SUPPLY = 550mA
-17.2V SUPPLY = 50mA

NOTES:

1. L GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS;
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR
INTEGRATED CIRCUITS

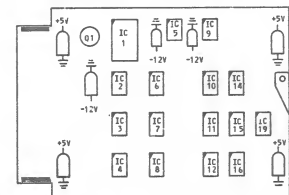
IC CODE	BAT. TERM.	GRD TERM.
472C	16	7, 8
410P	16	8
472C	16	7
410CJ	16	8
41M	16	8
555A	1, 2	5
5550C	8	4
KS-2070, L1	16	8
2033B	8	4

4. BATTERY AND GROUND TERMINALS FOR
THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000, 119
GRD	200, 319

5. HORIZONTAL MOUNTING CENTERS AT
1.0 INCH.

6. INTEGRATED CIRCUIT AND TRANSISTOR LOCATION GUIDE:
(COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK13
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (HIGHER SERIES IS ACCEPTABLE.)	
ACCEPTABLE SERIES	1, 2

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING
ONLY THOSE SHEETS AFFECTED WILL BE
REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND
BROUGHT UP TO DATE EACH TIME ANY SHEET
OF THE DRAWING IS REISSUED, OR A NEW
SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED
OR NEW SHEET WILL BE THE SAME ISSUE
NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN
THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET
INDEX IS RECOGNIZED AS THE LATEST ISSUE
NUMBER OF THE DRAWING AS A WHOLE.

NOTICE— NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL
SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.ISSUE
3D1

JK13 CIRCUIT PACK

BUFFER 0
CIRCUITBELL TELEPHONE LABORATORIES
INCORPORATED

2

CPS-JK13
3 SHEETS

65

CPS-JKT



PART OF CS JK13

BUFFER 0

COMPONENT LIST
INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 535X ②	IC2 41BP	IC3 -1CA	IC4 41CJ	IC5 3990C (FAIRCHILD) 2833B (SYNTEK) ①	IC6 KS-2467B, LI SHARP-T.T.	IC7 41CJ	IC8 41CJ	IC9 3990C (FAIRCHILD) 2833B (SYNTEK) ①
A	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC
B	WREG 289	WFLCLO 282	SDRT0 267	CH10B 201	BUFD 205	MTXB 2F5	CH10A 2C1	CH10C 2E1	BUFT 284
C		WFLCLK1 2C2	BA16CH 2E2						
D		CLC00 280	BAC10 265						
E		LD01 2C4							
F		SD1N1 2C3							
G		FACT1 2C5							

LOC CODE ELEM ID	IC10 41BP	IC11 41AE	IC12 41W	IC14 KS-2467B, LI SHARP-T.T.	IC15 41CJ	IC16 41CJ	IC19 41CJ
A	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC
B	B1, BU10 2E4	SP2 265	CARY00 2F1	MTXA 202	CH11A 2C8	CH11C 2E8	CH11B 208
C	BD, BU10 2E6	SDRT1 265	CARY01 2G1				
D	CLC10 287		CARY10 -F7				
E	CLC11 2F1		CARY11 267				
F	CLC10 2E2						
G	CLC10 2F2						
H	CLC10 2E2						

CAPACITOR

DESIG	CODE
[2] C1, C2	① 100K, 1
C3	② 100K, 1
C4	③ KS-1977A L1, 0.01
C5	④ 100K, 1
[4] C7-C10	⑤ KS-1977A L1, 0.01
[16] C11-C26	⑥ KS-1977A L1, 0.01

DIODE

DESIG	CODE
CRT	① 444M

RESISTOR

DESIG	CODE
R1	① KS-20616 L1A, 100
R2	392
R3	432
R4	160
R5	KS-20616 L1A, 100

TRANSISTOR

DESIG	CODE
Q1	① 2N1

CIRCUIT DESCRIPTION:

THIS CIRCUIT PACK IS PART OF THE BUFFER UNIT. THE 1024-BIT SHIFT REGISTERS, BUFO AND BUFI, PROVIDE SERIAL DATA STORAGE. EACH SHIFT REGISTER HAS ASSOCIATED WITH IT A 16-BIT COUNTER. THE COUNTERS INCREMENT EACH TIME THAT THE ASSOCIATED BUFFER IS CLOCKED. THE TWO BUFFERS CAN BE INDEPENDENTLY CLOCKED DUE TO THE MULTIPLEXING OF CLOCK AND DATA INPUT SIGNALS.

WHEN LEAD 1ACT0 IS LOW, BUFI IS CONSIDERED TO BE IN-LINE AND BUFO IS CONSIDERED TO BE OFF-LINE. IN-LINE CLOCK PULSES AT INPUT WFLCLO ARE ROUTED THROUGH MTXA AND SHIFT THE DATA IN LEAD SD10 INTO BUFI'S DATA PORT D2. THE SELECT LEAD SEL BN BUFI IS HIGH AND THE DATA AT BUFI'S DATA INPUT PORT D1 IS IGNORED. THE OUTPUT DATA OF BUFI IS ROUTED THROUGH MTXB AND F1F SDRT1 AND APPEARS IN LEAD SDRT0.

BUFI IS CLOCKED ON THE TRAILING EDGE OF THE PULSE ON LEAD WFLCLO AND F1F SDRT1 IS CLOCKED ON THE LEADING EDGE. THE 1024-BIT CARRY OF COUNTER 1 IS ROUTED THROUGH MTXB AND APPEARS IN BAC10. THE 16-BIT CARRY OF COUNTER 1 APPEARS IN LEAD BAC10. BAC10 AND BAC10 ARE GATED WITH THE IN-LINE CLOCK PULSE AND THEREFORE ARE AS WIDE AS THE GATING LEVEL PULSE ON LEAD WFLCLO.

AS LONG AS LEAD 1ACT0 IS AT GROUND LEVEL, BUFO IS CONSIDERED TO BE OFF-LINE. OFF-LINE CLOCK PULSES ON LEAD WFLCLO ARE ROUTED THROUGH MTXA AND SHIFT THE DATA ON LEAD L000 INTO BUFO'S DATA INPUT PORT D2. THE SELECT LEAD SEL BN BUFO IS HIGH AND THE DATA AT BUFO'S DATA INPUT PORT D1 IS IGNORED. THE OUTPUT DATA OF BUFO IS ROUTED THROUGH MTXB AND APPEARS IN LEAD SD10. THE 1024-BIT CARRY OF COUNTER 0 IS ROUTED THROUGH MTXB AND APPEARS IN LEAD SD10. THE 16-BIT CARRY OF COUNTER 0 IS ROUTED THROUGH MTXB AND APPEARS IN LEAD SD10.

WHEN LEAD 1ACT0 IS HIGH, BUFI IS IN-LINE AND BUFI IS OFF-LINE. IN THIS STATE IN-LINE CLOCK PULSES SHIFT THE DATA ON LEAD SD10 INTO BUFO AND OFF-LINE CLOCK PULSES SHIFT THE DATA ON LEAD L000 INTO BUFI.

A HIGH LEVEL ON LEADS CLC01 AND CLC11 CLEARS COUNTERS CH10 AND CH11 RESPECTIVELY. THE CLEAR FUNCTION OVERRIDES THE COUNTERS CLOCK INPUTS, AS LONG AS CLEAR IS ACTIVE, ANY CLOCK PULSES TO THE COUNTER ARE IGNORED.

WREG AND TRANSD10 PROVIDE A -12V REGULATED SUPPLY VOLTAGE FOR THE MOS SHIFT REGISTERS BUFO AND BUFI ON SERIES 1 CIRCUIT PACKS.

JK13 CIRCUIT PACK

CPS-JK13
SHEET 3

BELL TELEPHONE LABORATORIES

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3D1